

# First International Computer, Inc

## Portable Computer Group HW Department

Board name : Mother Board Schematic

**Project** : MR053+

**Version** : 0.1

**Date** : 01-12-2007

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Manager Sign by : JOE

Total confirm by : AVERY

Drawing by : Tom & Vicky

# 1. Schematic Page Description :

MR052 Schematic Ver :A

- |                              |                           |                              |
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| 12. Calistoga Host(1/6)      | 34. Headphone & SPDIF     |                              |
| 13. Calistoga DMI/Graph(2/6) | 35. SATA & CD ROM CNN     |                              |
| 14. Calistoga DDRII(3/6)     | 36. BCM4401 10/100 LAN    |                              |
| 15. Calistoga Power(4/6)     | 37. USB CNN ON-BRD        |                              |
| 16. Calistoga Power(5/6)     | 38. MDC & LED Indicator   |                              |
| 17. Calistoga Ground(6/6)    | 39. Reset Circuit         |                              |
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| 19. DDRII SDRAM SO-DIMM0     | 41. KBC KB3882 & GP CN    |                              |
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| 22. ICH7m CPU/IDE/SATA(2/4)  | 44. BLANK                 |                              |

## 2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI (Wireless LAN)
AD27	CardBus (RC832)
AD29	Lan (BCM4401)

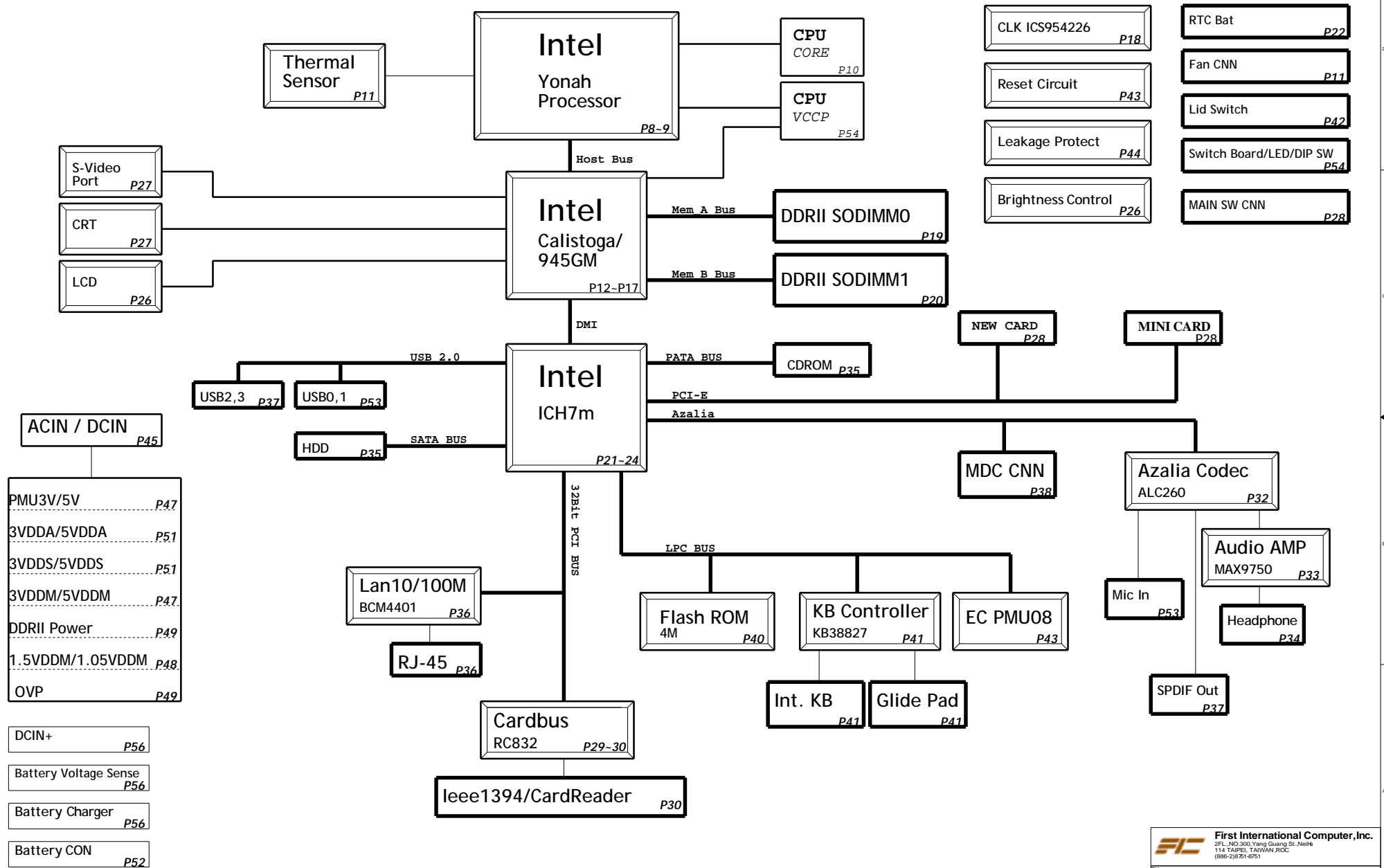
PCIINT	CHIP
IRQA	CardBus (RC832)/Lan (BCM4401)
IRQB	CardBus (RC832)/Mini PCI
IRQC	CardBus (RC832)/Mini PCI
IRQD	

BUSMASTER	REQ	CHIP
	REQ0 / GNT0	Lan (BCM4401)
	REQ1 / GNT1	CardBus (RC832)
	REQ2 / GNT2	Mini PCI (Wireless LAN)
	REQ3 / GNT3	
	REQ4 / GNT4	

IRQ Channel	Description
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Cascade)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	FLOPPY DISK
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

### 3. Block Diagram :



## 4. Nat name Description :

### Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#

VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

### Part Naming Conventions






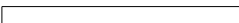
C	= Capacitor
CN	= Connector
D	= Diode
F	= Fuse
L	= Inductor
Q	= Transistor
R	= Resistor
RP	= Resistor Pack
U	= Arbitrary Logic Device
Y	= Crystal and Osc

### Net Name Suffix

#	= Active Low signal
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## 5. Board Stack up Description

### PCB Layers

L 1		Component Side, Microstrip signal Layer
L 2		Power Plane
L 3		Stripline Layer (AGTL,CLOCK,DDR)
L 4		Stripline Layer (Analog,LVDS,other)
L 5		Ground Plane
L 6		Solder Side, Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

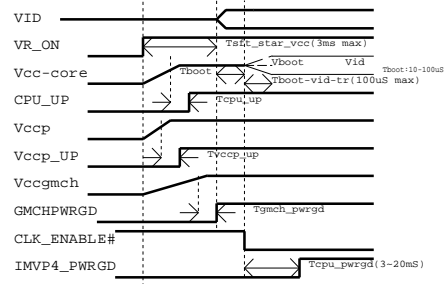
Power Rail	Destination	Voltage	SO Current
VCC_CORE	Yonah HFM: LFM:	1.3319V~1.4375V~1.4591V 0.9221V~0.9625V~0.9739V	36A
1.05VDDM	Yonah: AGTL+ termination 945GM: Core 945GM: AGTL+ termination ICH7m:	0.997V~1.05V~1.102V 1.0V~1.05V~1.1V 0.9475V~1.05V~1.1025V	2.5A 4.6A 1.4A
1.5VDDM	Yonah PLL 945GM: PCIE 945GM: LVDS 945GM: TVDAC 945GM: Various PLLS analog supply 945GM: DDR DLLS,DDRII,FSB HSIO ICH7m: ICH7m: ICH7m: ICH7m: Mini Card: Express Card:	1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V	120mA 1.5A 60mA 24mA 320mA 1.885A
1.8VDDS	945GM: DDRII System Memory SO-DIMM:	1.7V~1.8V~1.9V	3.1A
0.9VDDT_DDRII	DDRII Terminator:	0.855V~0.9V~0.945V	1.0A
2.5VDDM	945GM: PCIE analog 945GM: LVDS analog 945GM: LVDS I/O 945GM: CRT DAC CH7307:	2.32V~2.5V~2.625V 2.375V~2.5V~2.625V 2.375V~2.5V~2.625V 2.32V~2.5V~2.625V	2mA 10mA 60mA 70mA
3VDDM	945GM: HV CMOS 945GM: TVDAC analog ICH7m: ICH7m: ICH7m: ICH7m: ICH7m: Mini Card: Express Card: CLK Generator: ICS954226 Mini PCI: WirelessLan KBC: KB3886 Flash ROM: BIOS Azalia Codec: ALC260 Azalia MDC: HDD: SATA	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V	40mA 120mA
3VDDS	CardBus: TI PCI7411 CardBus: Slot voltage Lan: Broadcom BCM4401 Card Reader: SD/MMC/MS Azalia MDC: For wake up Mini PCI: For wake up	3.0V~3.3V~3.6V	
3VDDA	ICH7m: ICH7m: ICH7m: LCD:	3.0V~3.3V~3.6V	1.0A
5VDDM	Mini PCI: Azalia Codec: ALC260 Azalia MDC: HDD: SATA ODD: PATA Audio AMP: G1420 Woofer AMP: LM4991 Inverter:	3.0V~3.3V~3.6V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA Max: 1.8A ; R/W: 900mA ; STDBY: 45mA
5VDDS	CardBus: Slot voltage USB: x 4 ports	5V	2.0A
PMU3V	EC: PMU08 ICH7m: RTC		

## 6.Schematic modify Item and History :

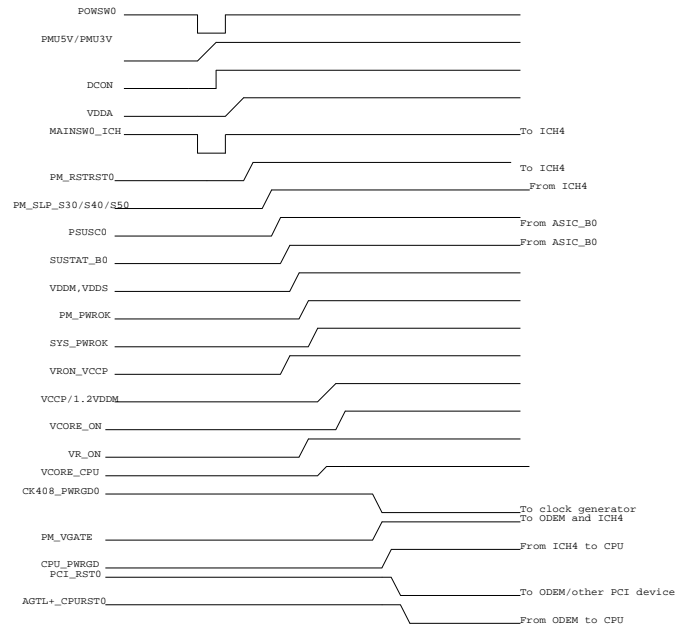
1025  
R479 change from 150ohm(NU) to 75ohm(NU)

# 7. power on & off & S3 Sequence :

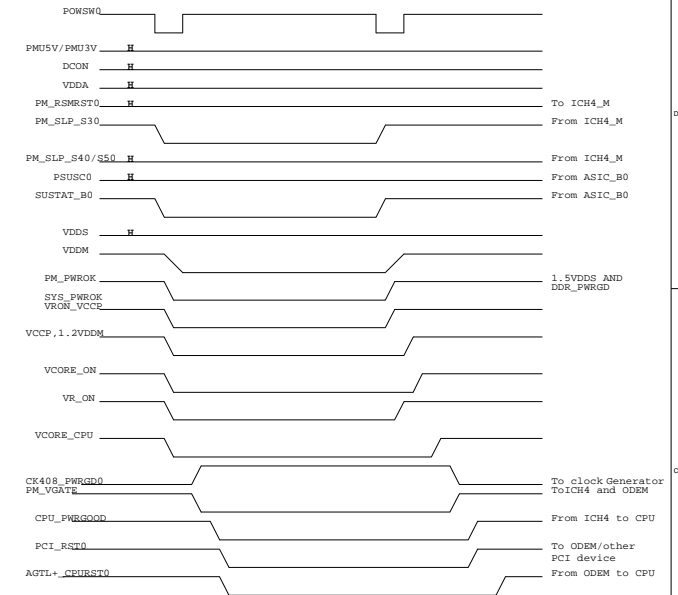
IMVP6 Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



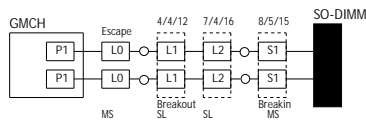
# 8. Layout Guideline :

## Calistoga (945GM) DDRII Layout Guidelines

### DDRII Signal Groups

Group	Signal Name	Length Matching and Length Formulas
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DQS[7..0]/SB_DQS[7..0]	
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#	
Control	SM_CKE[3..0] SM_ODT[3..0]	
Clock	SM_CLK[3..0] SM_CK[3..0]	
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#	

### CLK group : SM\_CLK[3..0], SM\_CK[3..0]



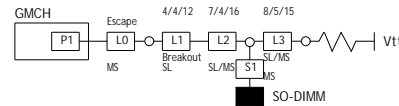
Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching (Total Length)	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exception s (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 2 00 mils

### Feedback group :

SA\_RCVENIN#, SA\_RCVENOUT#, SB\_RVENIN#, SB\_RCVENOUT#

These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

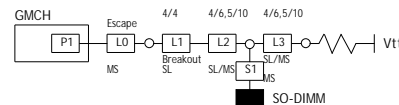
### Control group : SM\_CKE[3..0], SM\_CS#[3..0], SM\_ODT[3..0]



Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CTRL <= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

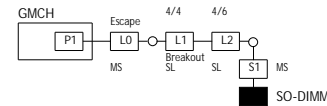
### Command group :

SA\_MA[13..0], SB\_MA[13..0], SA\_BS[2..0], SB\_BS[2..0], SA\_RAS#, SB\_RAS#, SA\_CAS#, SB\_CAS#, SA\_WE#, SB\_WE#



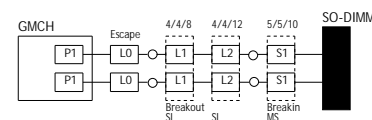
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CMD <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

### Data group : SA\_DQ[63..0], SB\_DQ[63..0], SA\_DM[7..0], SB\_DM[7..0]

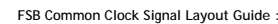
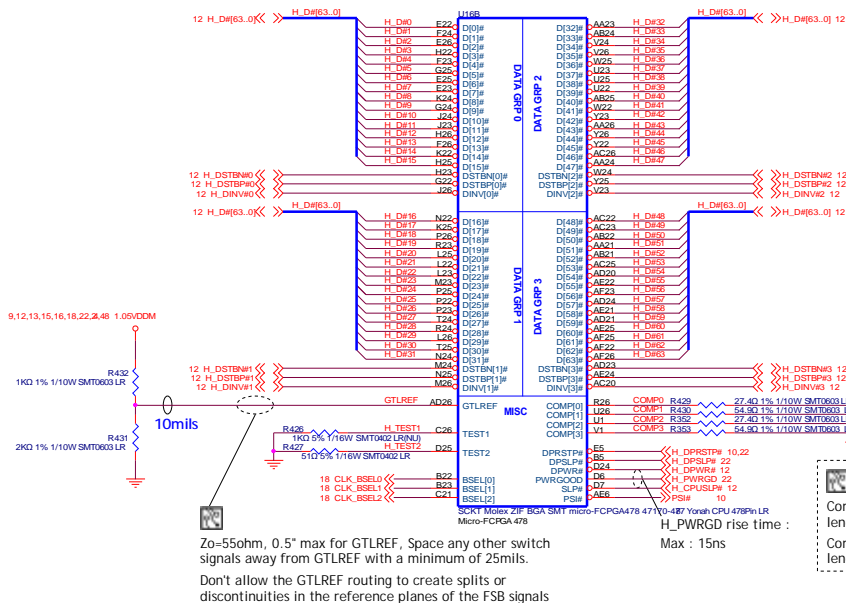


Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to (SDQS - 200mils) +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

### Data Strobe group : SA\_DQS[7..0], SA\_DQS#[7..0], SB\_DQS[7..0], SB\_DQS#[7..0]



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") <= DQS <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 2 00 mils



ADS# , BNR# , BPRI# , BRO# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

### FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0]_DINVO#	+/- 100 mils	DSTBP0#, DSTBN0#	+/- 25 mils
DATA#[31..16]_DINV1#	+/- 100 mils	DSTBP1#, DSTBN1#	+/- 25 mils
DATA#[47..32]_DINV2#	+/- 100 mils	DSTBP2#, DSTBN2#	+/- 25 mils
DATA#[63..48]_DINV3#	+/- 100 mils	DSTBP3#, DSTBN3#	+/- 25 mils

## FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data, Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

### FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

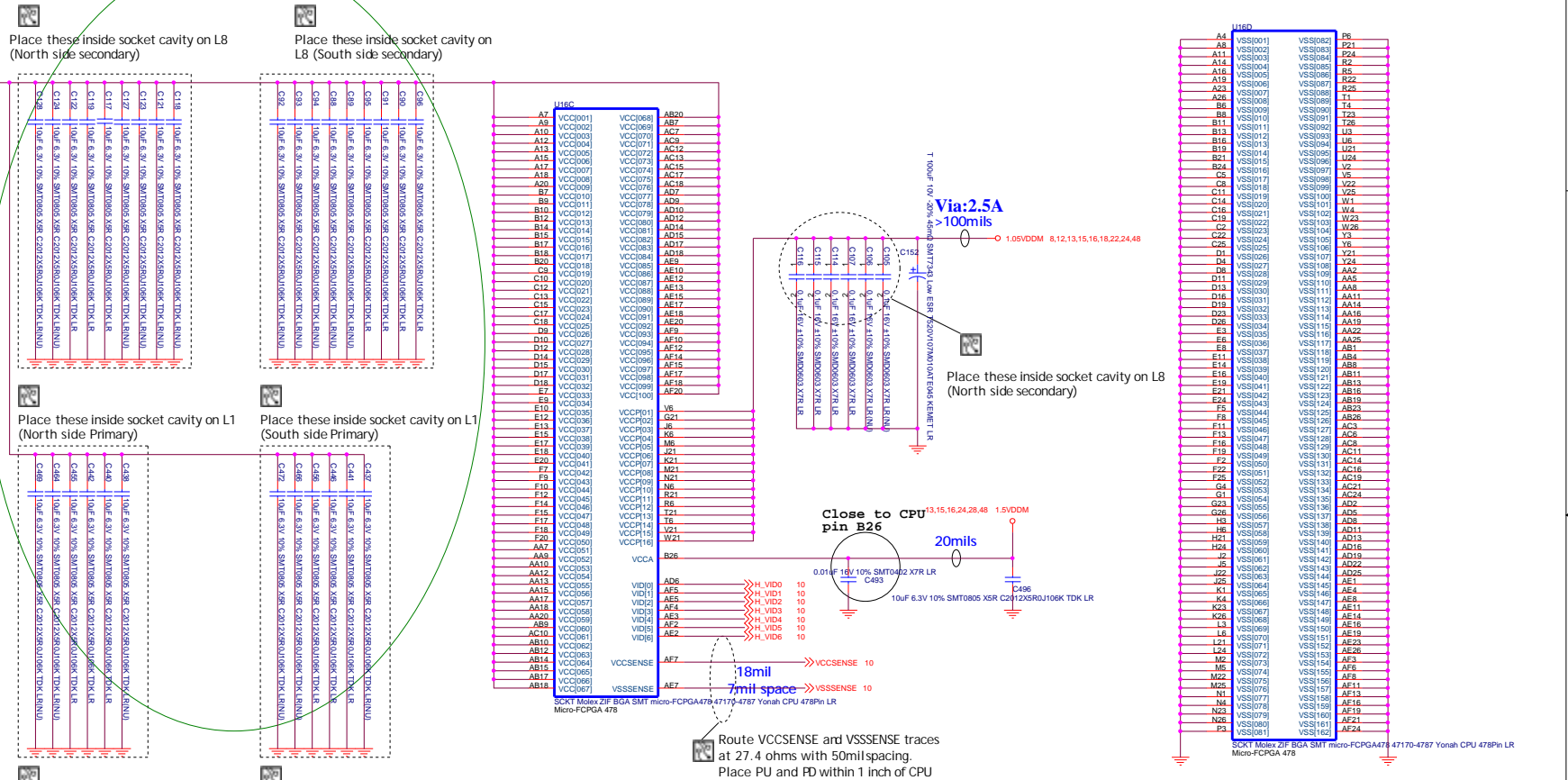
Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3], REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

\*\*\* No length matching requirements exist between ADSTB0# and ADSTB1#

### FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address[31..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
REQ[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
ADSTB[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils





IMVP IVLoad line slope : -2.1mV/A  
VCORE\_CPU 36A  
For Yonah CPU

Boost Voltage 1.2V  
Deeper Sleep Voltage 0.748V



Assume  $R_{18} = R_{in} = 1K \text{ Ohm}$

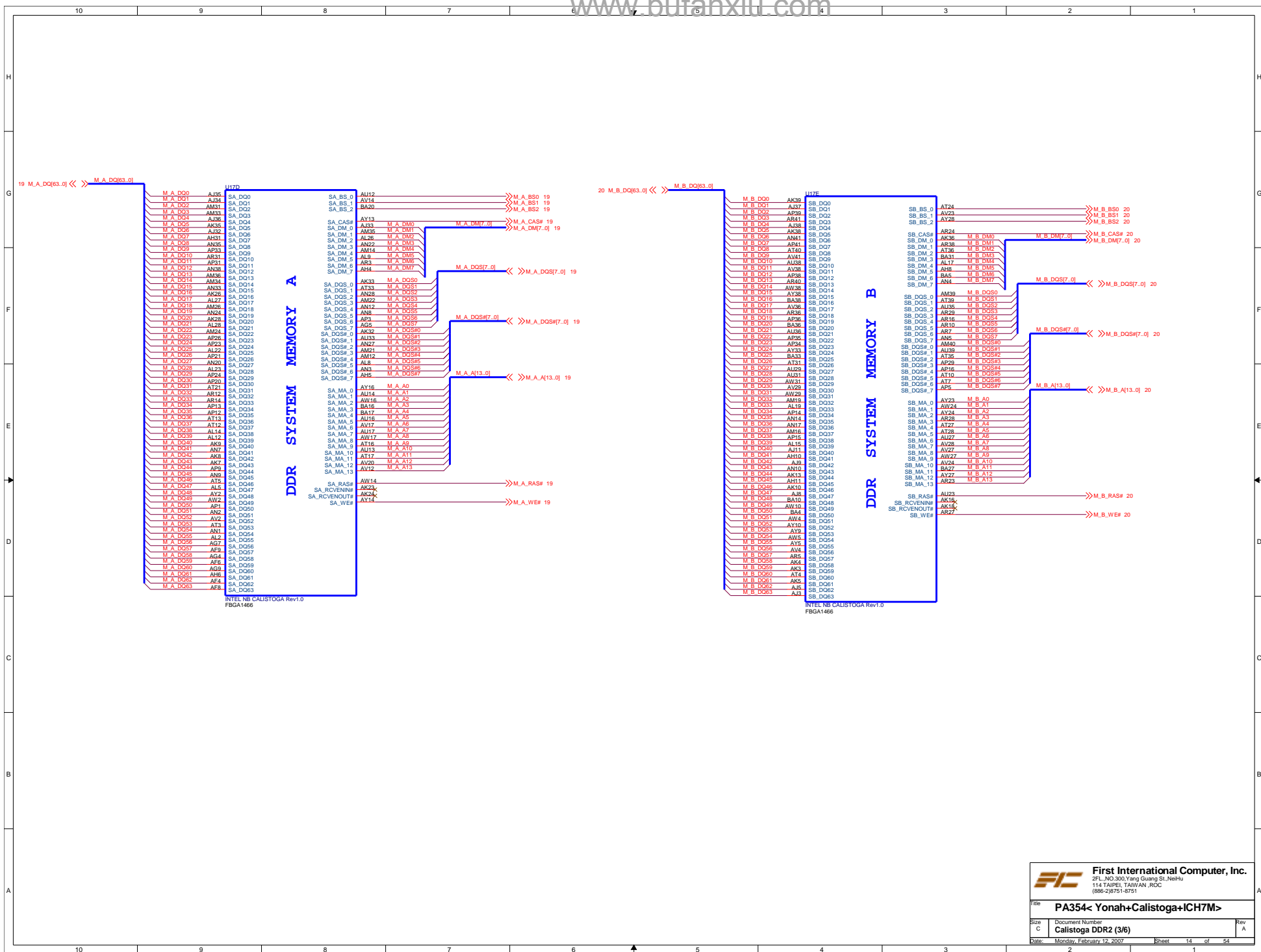
$R_{19} = R_{fb} = [N * R_{droop} / (DCR * G) - 1] * R_{in} = 5.69K \sim 5.11K$   
 $R_{droop} = \text{Intel spec. } -2.1m \text{ Ohms}$

$L / DCR = [R_n / R_S (\text{eqv})] * C_n$   
 $C_{782} * C_{783} C_n = L / DCR / [R_n / R_S (\text{eqv})] = 0.285uF$

[illegible]







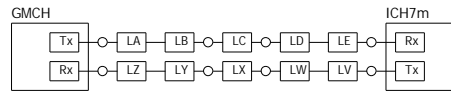








## DMI Routing Guideline



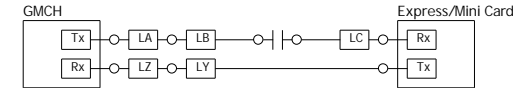
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

\*\*\* When routing near the edge of their reference plane, trace should maintain at least 40 mils space to the edge of the plane

\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

## PCIe Routing Guideline



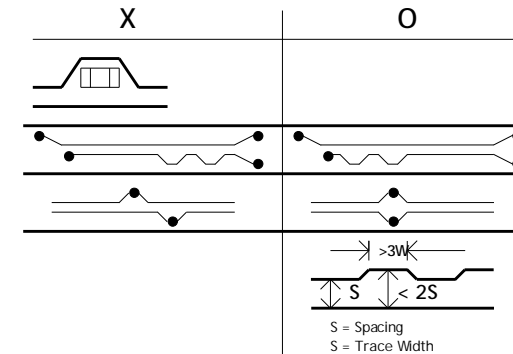
Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Pair Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

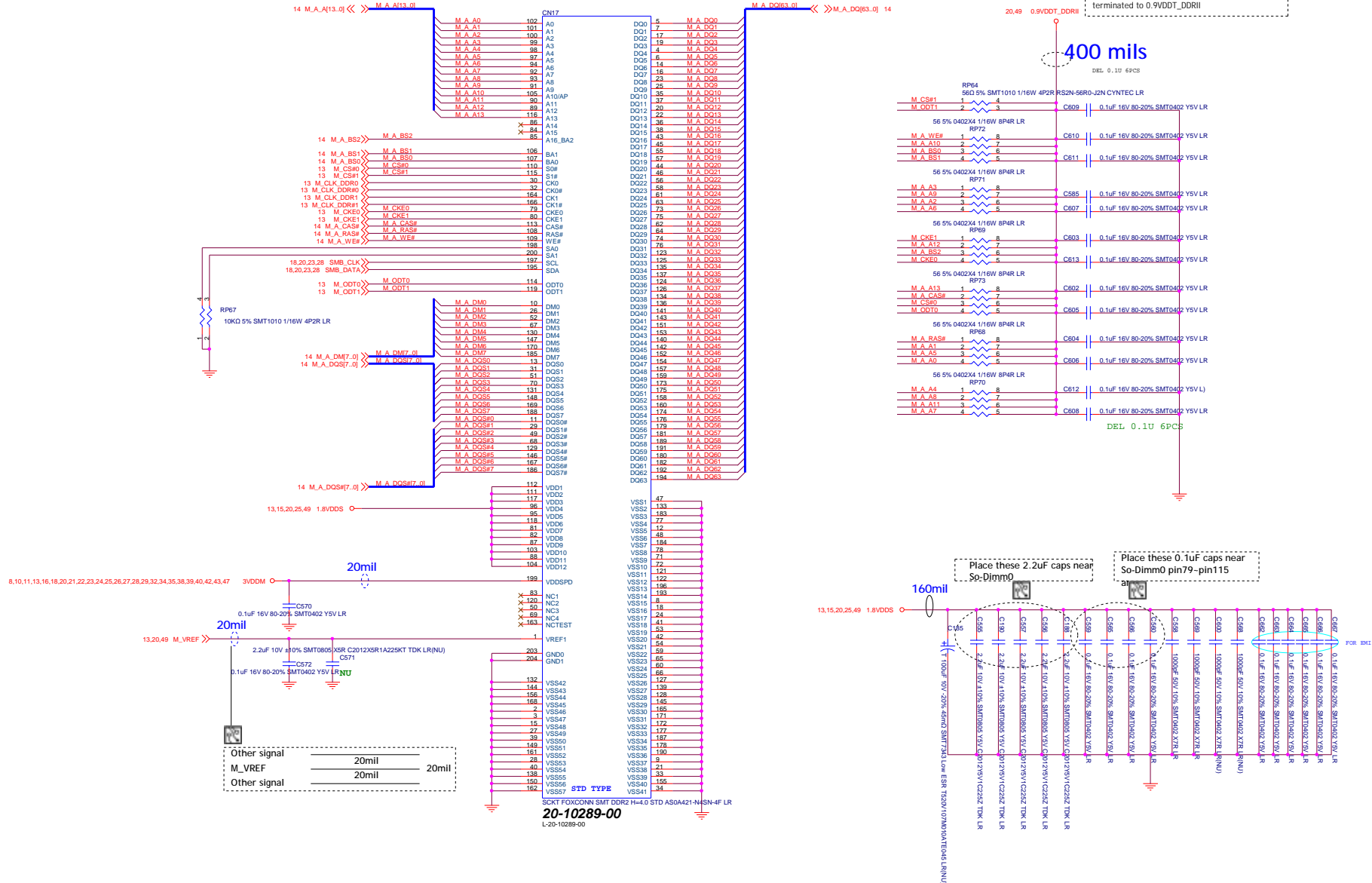
\*\*\* When routing near the edge of their reference plane, trace should maintain at least 40 mils space to the edge of the plane

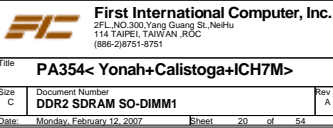
\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils





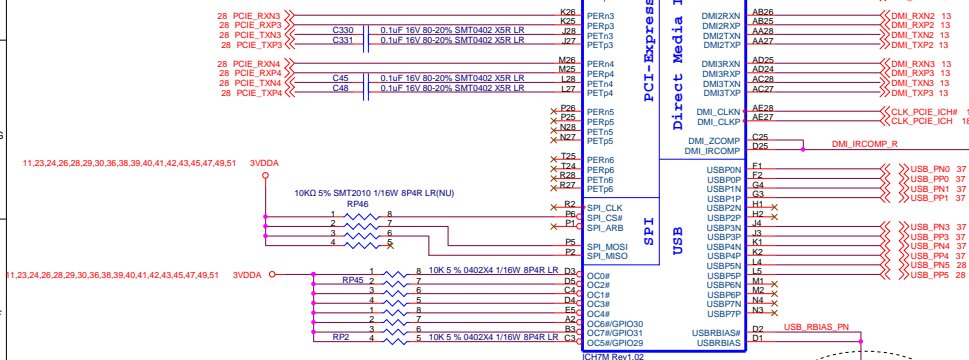
SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

***SO-DIMMO***



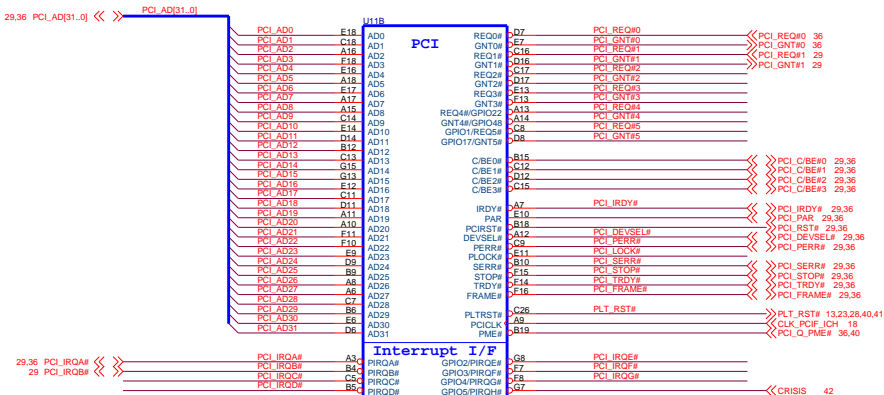
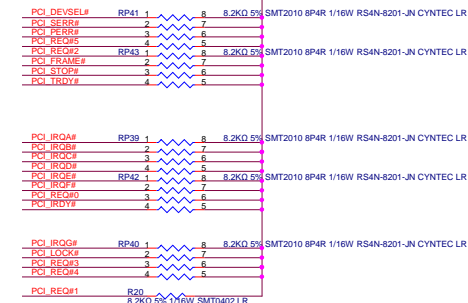


PCIe AC coupling caps need to be within 250mils of the driver



Place within 500mils of ICH  
5/5 mils spacing on microstrip

PCI Pull up



Buffer to reduce loading on PLT\_RST#

Check BIOS type

PCI\_GNT#3 No stuff: by default  
Stuff: For A16 swap override

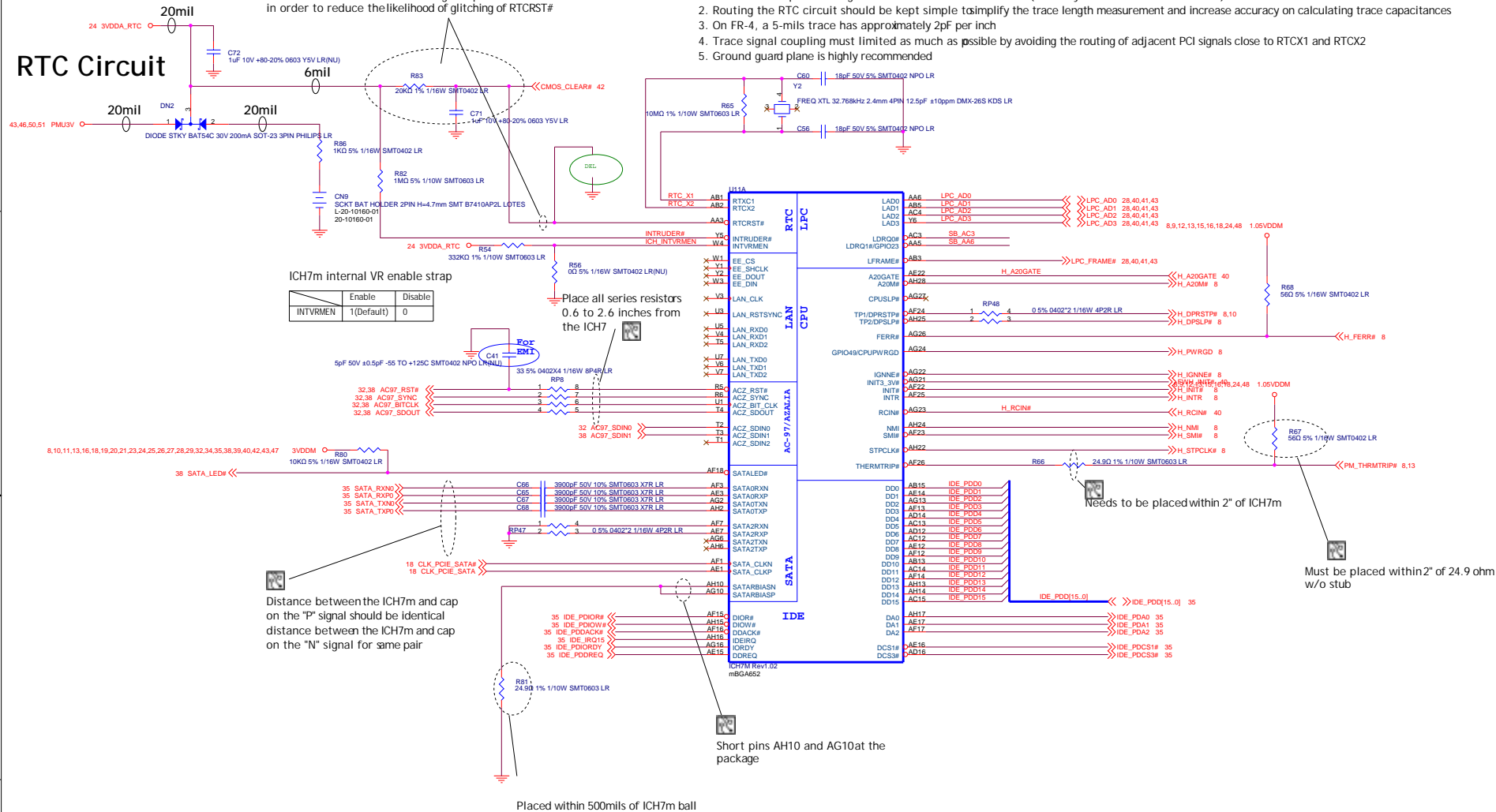
PCI_GNT#4	PCI_GNT#5	
1	1	LPC
0	1	PCI
1	0	SPJ

## RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that the larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#



1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



AC2\_SDATOUT strap functionality base on RSV9 strap  
XOR chain entrance (RSV9 pulled low)  
PCIe port config bit 1 (RSV9 not pulled low)

Stuff for XOR chain in testing

01, 11, 13, 16, 18, 19, 20, 21, 22, 24, 25, 26, 27, 28, 29, 32, 34, 35, 38, 39, 40, 42, 43, 47

ACZ\_SPKR No stuff: by default  
Stuff: for NO reboot

ICH\_SPKR R21 10KΩ 5% 1/16W SMT0402 L(R)N(U)

GPO27 R25 10KΩ 5% 1/16W SMT0402 LR

R24 0Ω 5% 1/16W SMT0402 L(R)N(U)

Default is 1-X  
Add 0ohm for BIOS  
Recovery

3VDDM

11,21,24,26,28,29,30,36,38,39,40,41,42,43,45,47,49,51 3VDDA

PM	R237	10K0 5% 1/6W SMT0402 LR(U)
EC	SC1W	10K0 5% 1/6W SMT0402 LR(U)
EC	R22	8.2K0 5% 1/6W SMT0603 LR
PCIE_WAKE#	R24	10K0 5% 1/6W SMT0603 LR
SMB_ALERT#	R241	10K0 5% 1/6W SMT0402 LR

8,10,11,15,16,18,19,20,21,24,25,26,27,28,29,32,34,35,38,39,40,42,43,47 3VDDM

PM	THRM2	8.2K0 5% 1/6W SMT0402 LR
PM	TEMP1	8.2K0 5% 1/6W SMT0402 LR

R6.11, 13, 16, 18, 20, 21, 22, 24, 25, 26, 27, 28, 29, 32, 34, 35, 38, 39, 40, 42, 43, 47 3VDD0

GPH039 R322 10KΩ 5% 1/6W SMT0402 LR

GPH07 R293 10KΩ 5% 1/6W SMT0402 LR

GPH10 R236 10KΩ 5% 1/6W SMT0402 LR

R274 R274 10KΩ 5% 1/6W SMT0402 LR

GPH15 R247 10KΩ 5% 1/6W SMT0402 LR

GPH08 R23 10KΩ 5% 1/6W SMT0402 LR

R262 R262 10KΩ 5% 1/6W SMT0402 LR

PCI\_SERIRQ R318 10KΩ 5% 1/6W SMT0402 LR

11, 21, 24, 26, 28, 29, 30, 38, 39, 40, 41, 42, 43, 45, 47, 49, 51 3VDDA

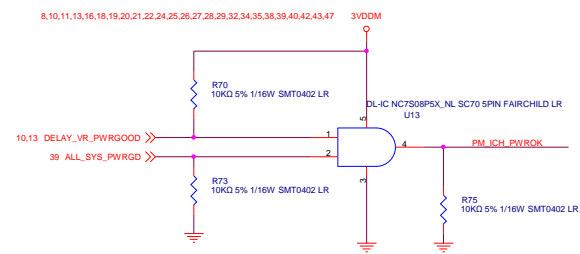
GPH12 R255 10KΩ 5% 1/6W SMT0402 LR

GPH08 R246 10KΩ 5% 1/6W SMT0402 LR

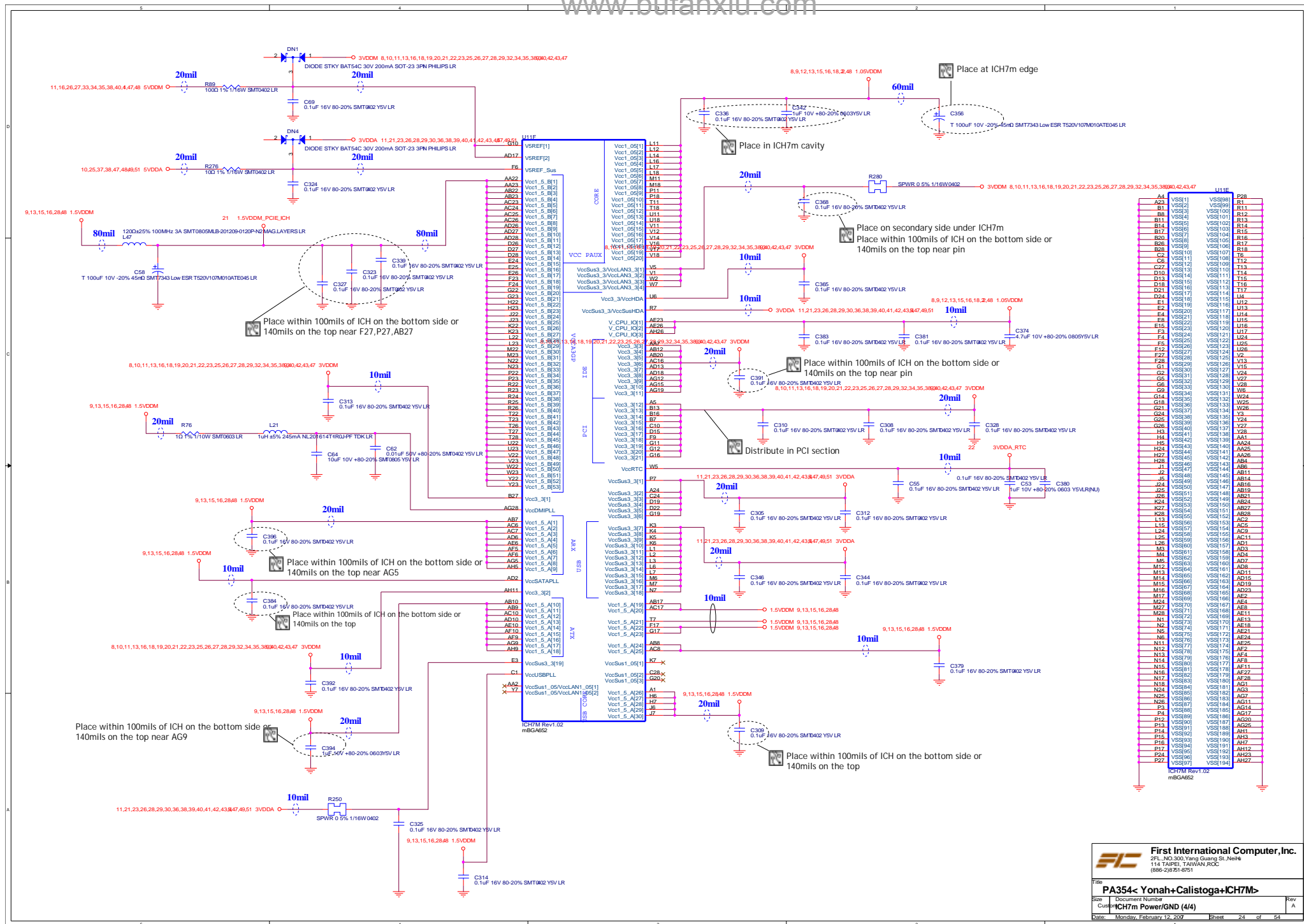
Q3 SWR R244 10KΩ 5% 1/6W SMT0402 LR

G2 R270 10KΩ 5% 1/6W SMT0402 LR

+









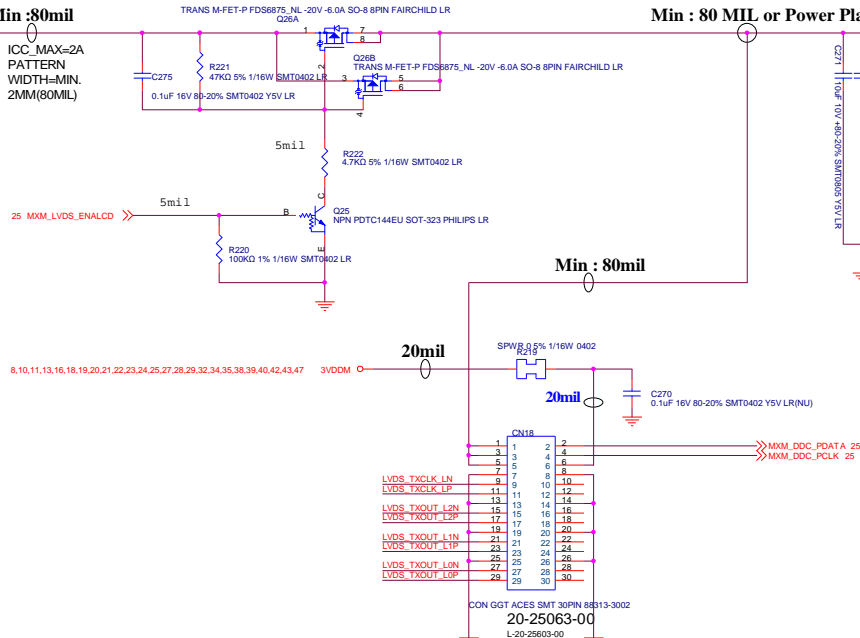
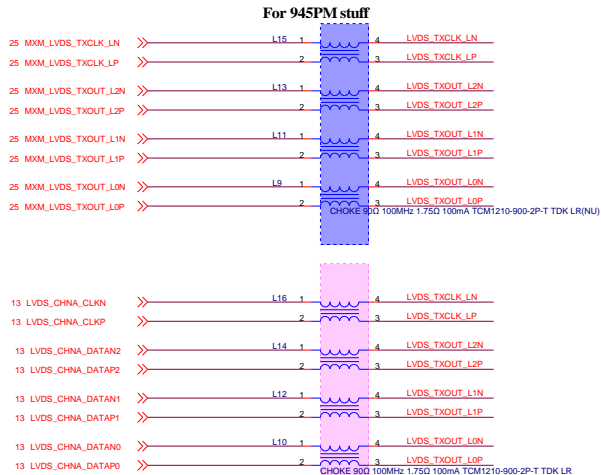


IF 945GM MOUNT L13-L16,L18-L21,  
UNMOUNT L132- L139,

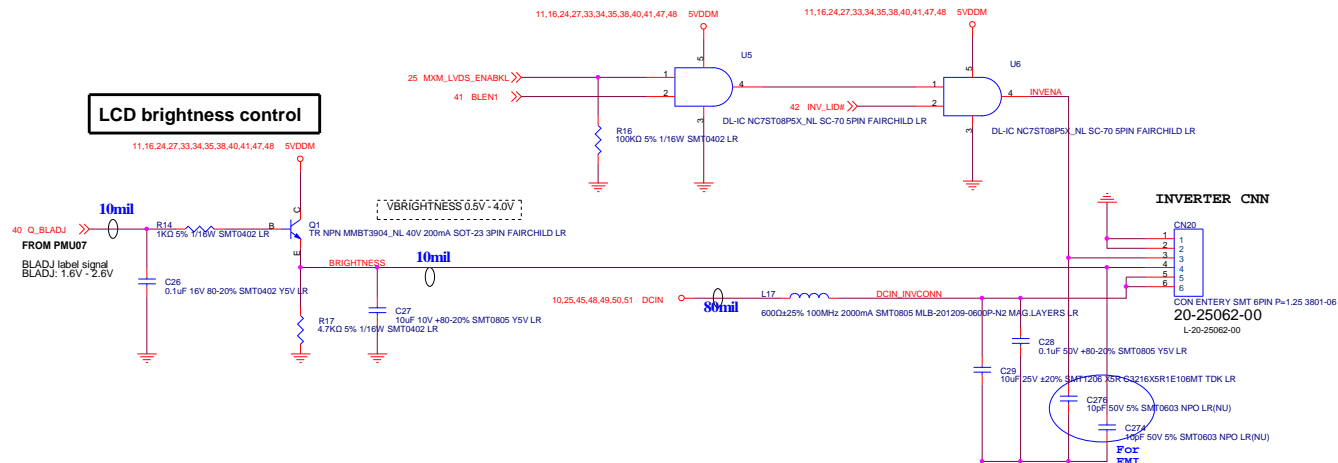
IF 945PM MOUNT L132-L139,  
UNMOUNT L13 - L16,L18-L21

Min :80mil

Min : 80 MIL or Power Plane



### LCD brightness control



FIC International Computer, Inc.  
17FL NO286, SEC.1, WENHWA 2nd RD. LINKOU HSIANG,  
244 TAIPEI, TAIWAN, ROC  
(886-2)2600-8818

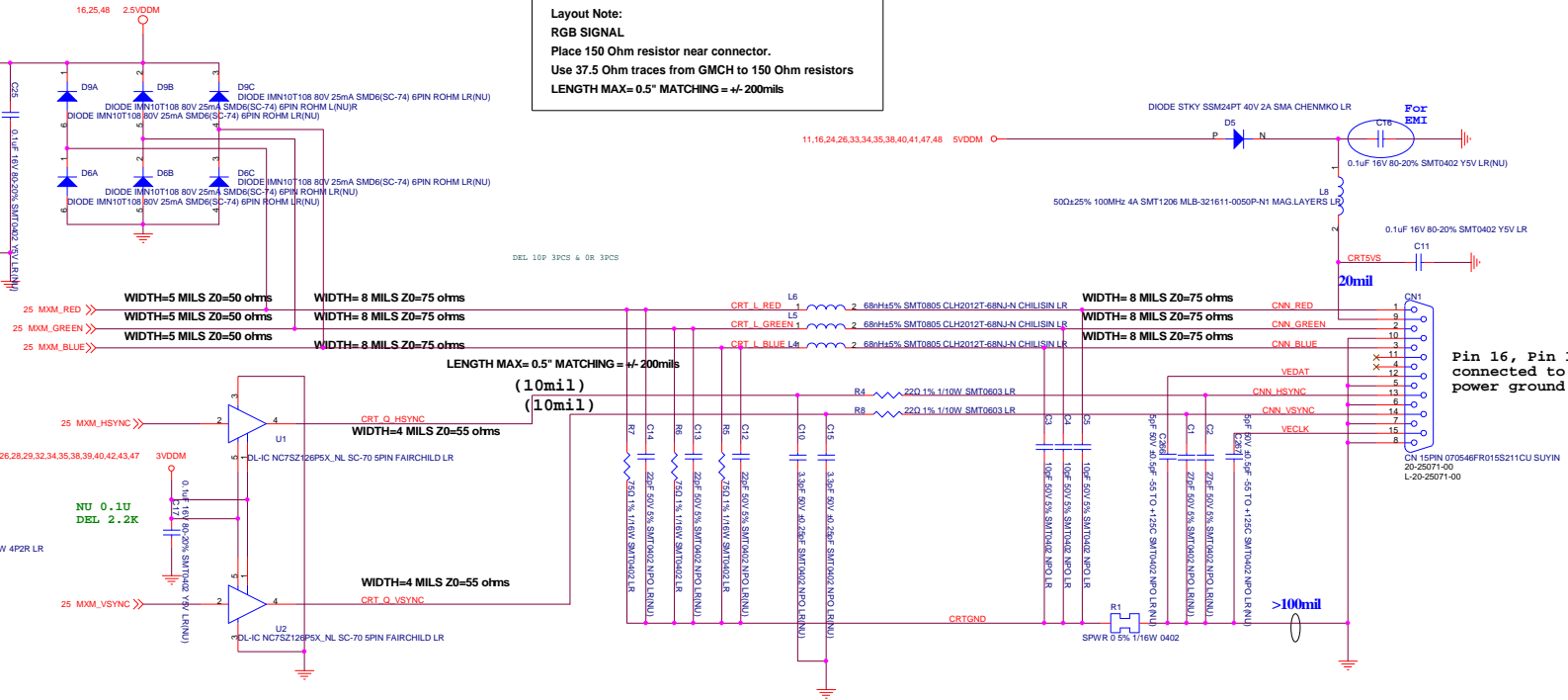
File	PA354c_Yonah+Calistoga+ICHTM>	Rev	A
Size	Document Number		
C	Panel I/F		
Date	Monday, February 12, 2007	Sheet	26 of 54

## CRT CIRCUIT

**Layout Note:**  
**RGB SIGNAL**  
 Place 150 Ohm resistor near connector.  
 Use 37.5 Ohm traces from GMCH to 150 Ohm resistors  
 LENGTH MAX= 0.5" MATCHING= +/-200mils

LAYOUT GUIDE

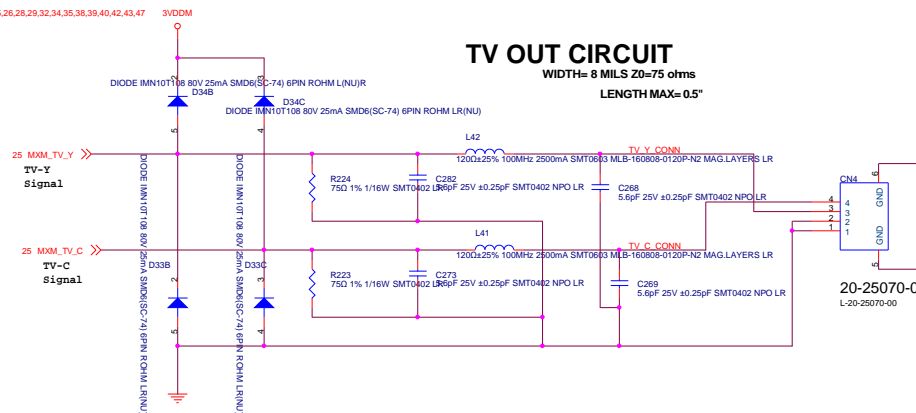
Other Signal  
 20 mil  
 MXM\_RED  
 20 mil  
 MXM\_GREEN  
 20 mil  
 MXM\_BLUE  
 20 mil  
 Other Signal

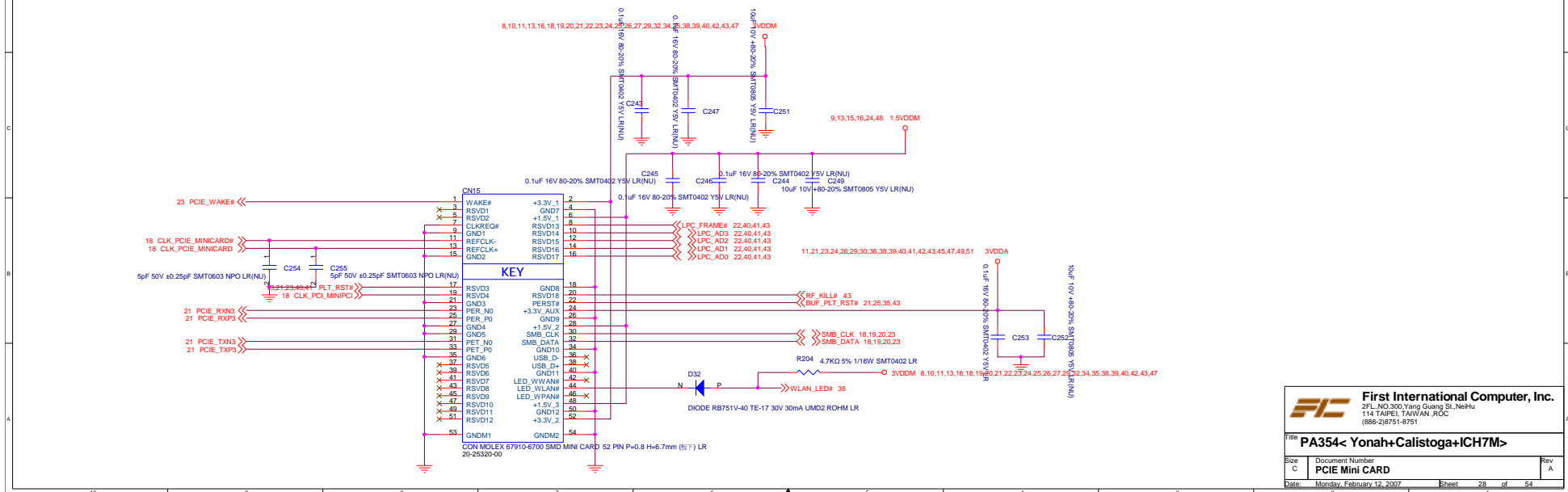


## TV OUT CIRCUIT

WIDTH= 8 MILS Z0=75 ohms  
 LENGTH MAX= 0.5"

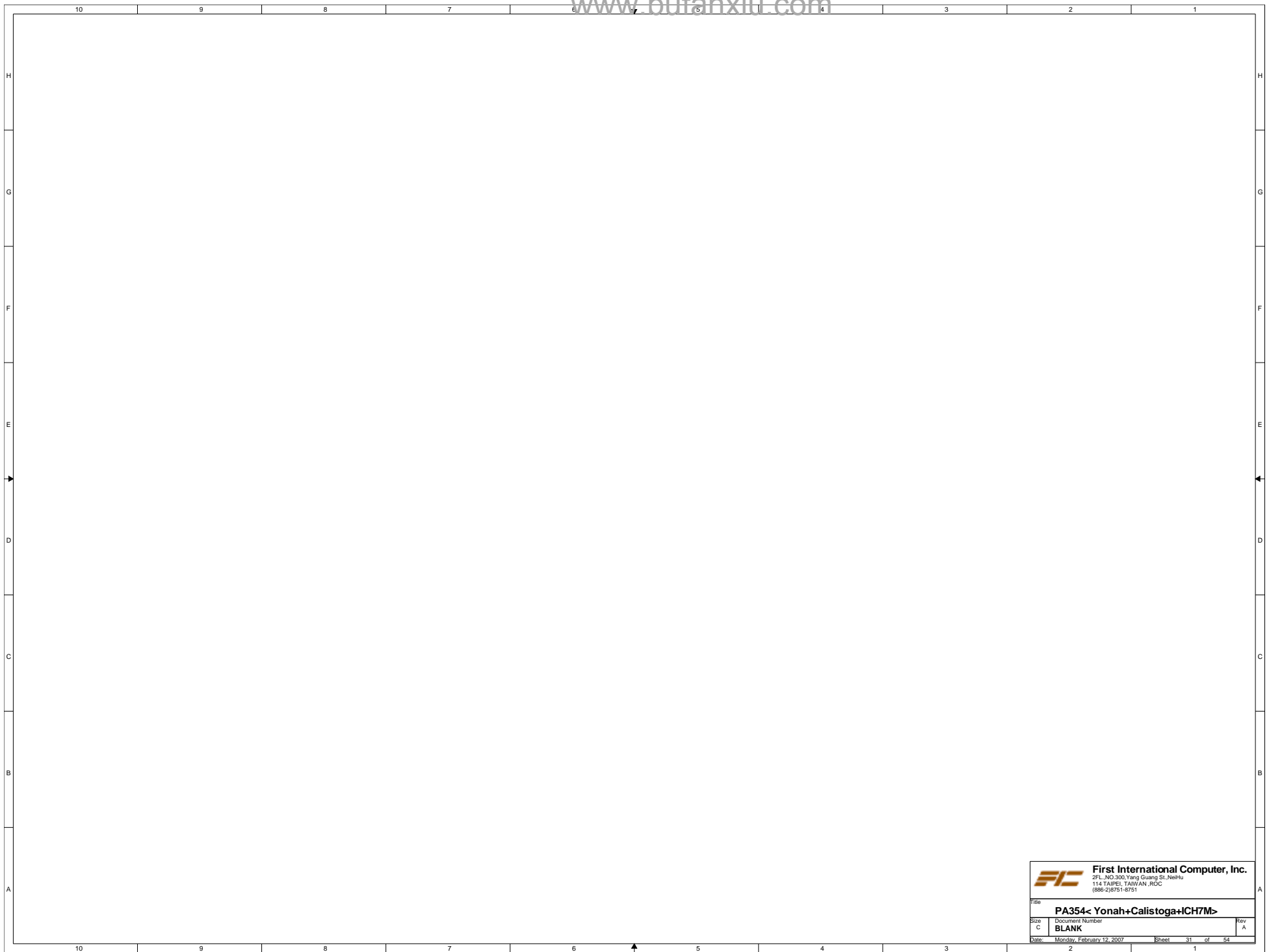
Place 150 Ohm resistor near connector.  
 Use 37.5 Ohm traces from GMCH to 150 Ohm resistors  
 WIDTH=5 MILS Z0=50 ohms




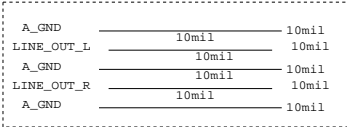




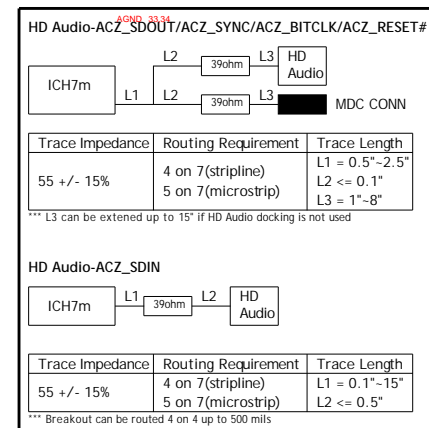




		<b>First International Computer, Inc.</b> 2F L. NO.300, Yang Guang St., NeiHu 114 TAIPEI, TAIWAN, ROC (886-2)8751-8751	
Title <b>PA354&lt; Yonah+Calistoga+ICH7M&gt;</b>			
Size C	Document Number <b>BLANK</b>		Rev A
Date: Monday, February 12, 2007		Sheet 31 of 54	



```
ADDR :57C0H bit 15 set:'1'
```

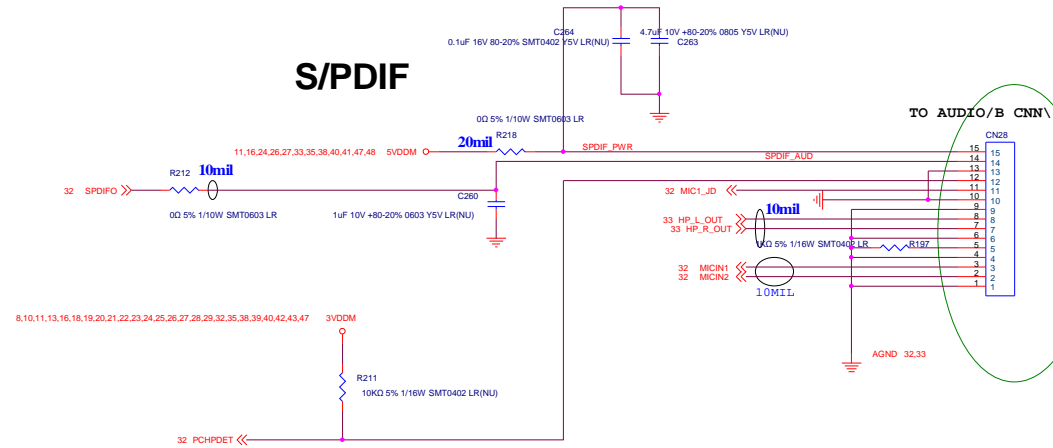


## AC97 CODEC Layout Guide:

1. Digital and analog ground should be tied at 2-3mm gap
2. All the analog trace routing should be over the analog ground plane
3. The analog and digital planes should electrically shorted at one place
4. Supply high frequency decoupling capacitors and high frequency decoupling filter caps must be routed on the same layer as the codec
5. Analog I/O routing should be kept as short as possible
6. All the I/O routing should be shielded with analog ground traces
7. Use of ground plane fill and the copper fill should be shorted to the analog ground plane
8. All the clock signal should be as short as possible
9. AC-link clock signal should have a series resistor close to the codec
10. The AC-link signal should be shielding with ground
11. Split analog and digital ground on the PCB
12. Analog signals only over analog ground plane
13. Digital signals only over digital ground plane
14. Circulate analog section away from high speed digital circuit
15. Place smallest bypass capacitor closest to IC pin
16. Use metal film resistors and NPO capacitors in analog path
17. Audio signal trace width is 12mil







10mil 10mil

10mil 10mil

10mil 10mil

AGND 10mil 10mil

LOUT+ 10mil 10mil

AGND 10mil 10mil

LOUT- 10mil 10mil

AGND 10mil 10mil

10mil 10mil

10mil 10mil

10mil 10mil

10mil 10mil

AGND 10mil 10mil

LINE\_OUT\_L 10mil 10mil

AGND 10mil 10mil

LINE\_OUT\_R 10mil 10mil

AGND 10mil 10mil

AGND

ROUT+

AGND

ROUT-

AGND

10mil 10mil

10mil 10mil

10mil 10mil

10mil 10mil

10mil 10mil

AGND 10mil 10mil

A\_HP\_L 10mil 10mil

AGND 10mil 10mil

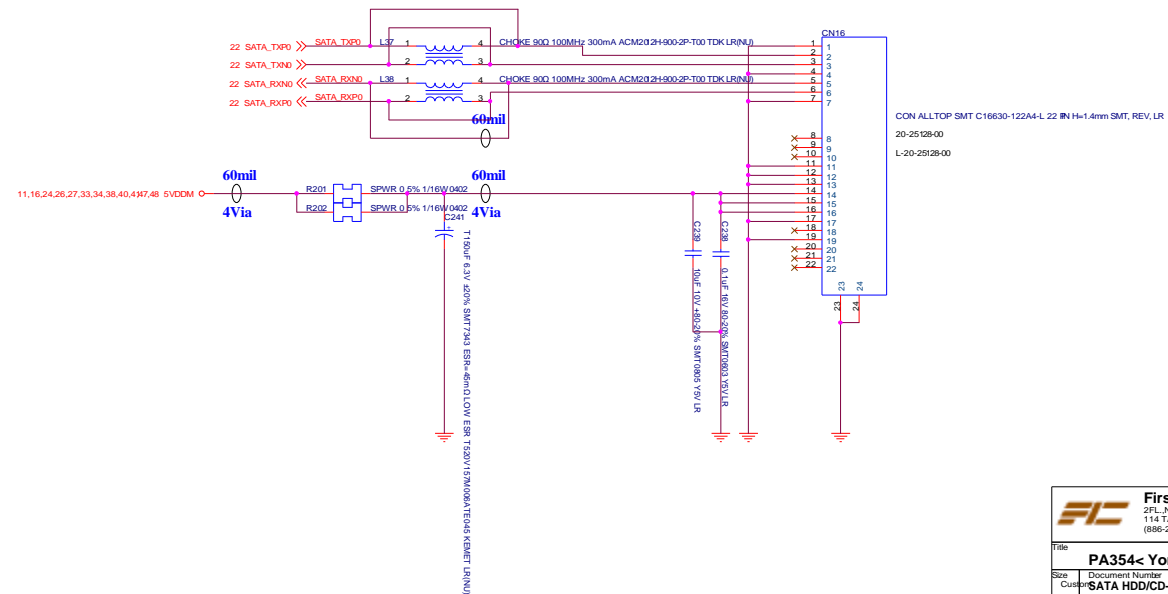
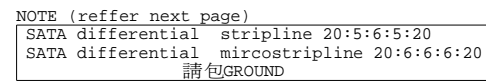
A\_HP\_R 10mil 10mil

AGND 10mil 10mil

GND\_POWER 10mil 10mil

SYS\_BEEP0/AC97\_PCBEEP 10mil 10mil

GND\_POWER 10mil 10mil



each signal trace between the CPU and the BJ45 should have a controlled impedance of 50 ohms. The distance between each pair coming from the same BCM4401E device should be 50 mils minimum. Differential pairs from different BCM4401E devices should have 200 mils spacing between them.

Route differential pairs such that the + and - signals are matched in length.(as short as possible)

Place the series termination resistors close to the source.

If any two traces must cross each other on different layers,always cross them at or near 90 degree to minimize potential crosstalk.

To place the power train resistors a minimum distance of 1.5 inches away from the BCM4401E device.

The BCM4401E clock so urce needs to be placed as close as possible to the BCM4401E device.

Connect the resistor as close to the RMC4 pin as possible, and keep the trace between them as short as possible.

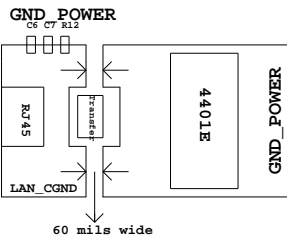
Avoid routing any high -speed signal traces in this area.

Bypass the power pins with low impedance surf ace mount capacitors connected directly into the power planes, as close as possible to the pins to reduce the parasitic inductance in series with the capacitor.

If vias cannot be placed next to the pins,then use 20 mils traces.

If power pins are next to each other and there is not much room to accommodate multiple capacitors,then the power pins can share the same capacitors.

Place the filtering circuit as close to the pin as possible.



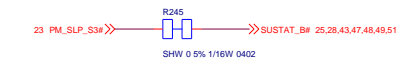
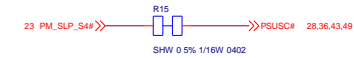
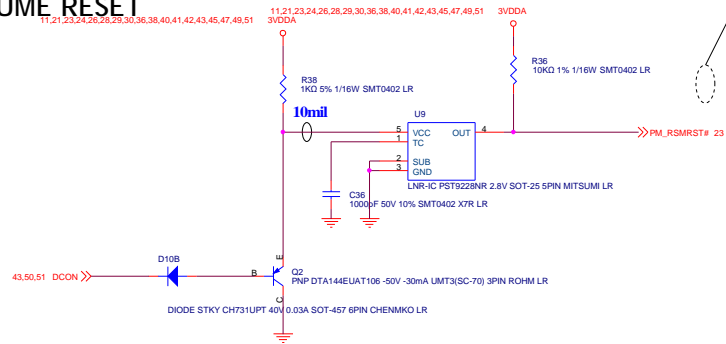
1. In addition, it is also important to keep the gap between Chassis GND and System GND to be wider than 60mils for better Isolation requirement.
2. The analog GND pins must maintain a good ground return path.
3. All 4 pairs trace width of 4pair is 4mil. It's 10mil between 2 trace(+/-), It's more than 50mil spacing different differential pairs.



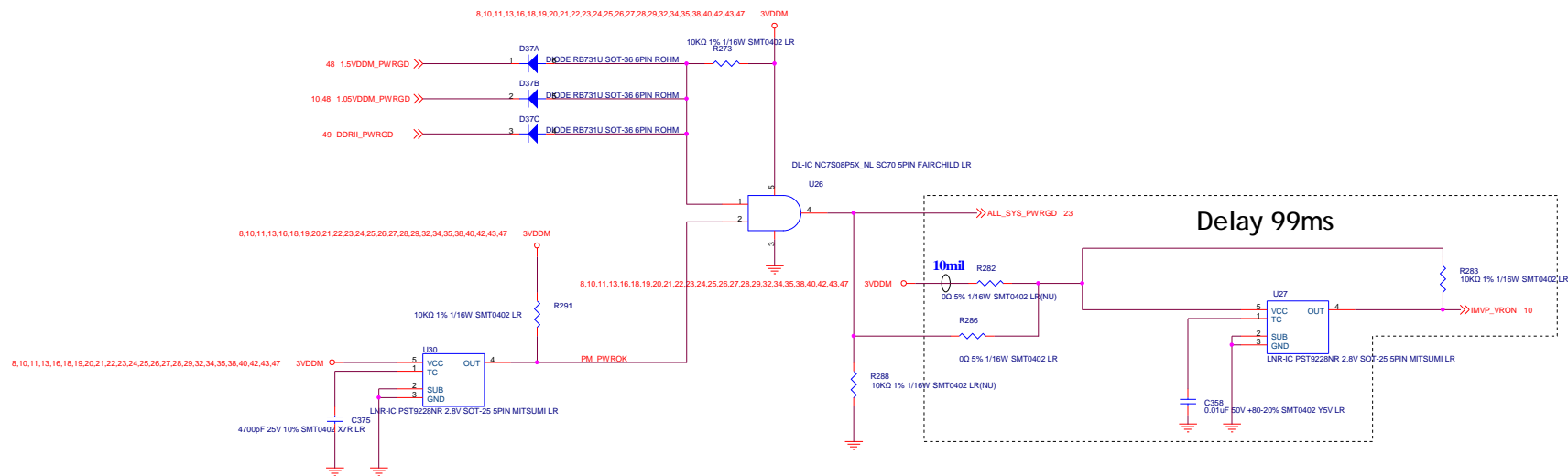
### LED indicator control logic

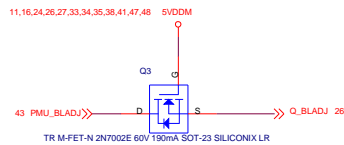
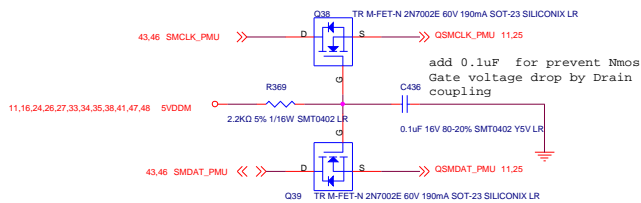
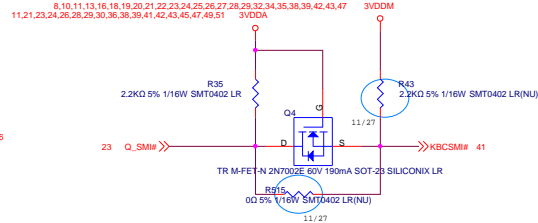
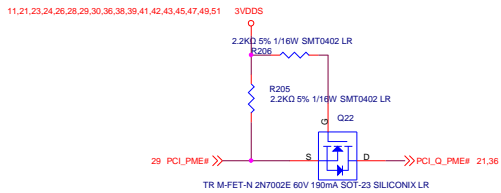
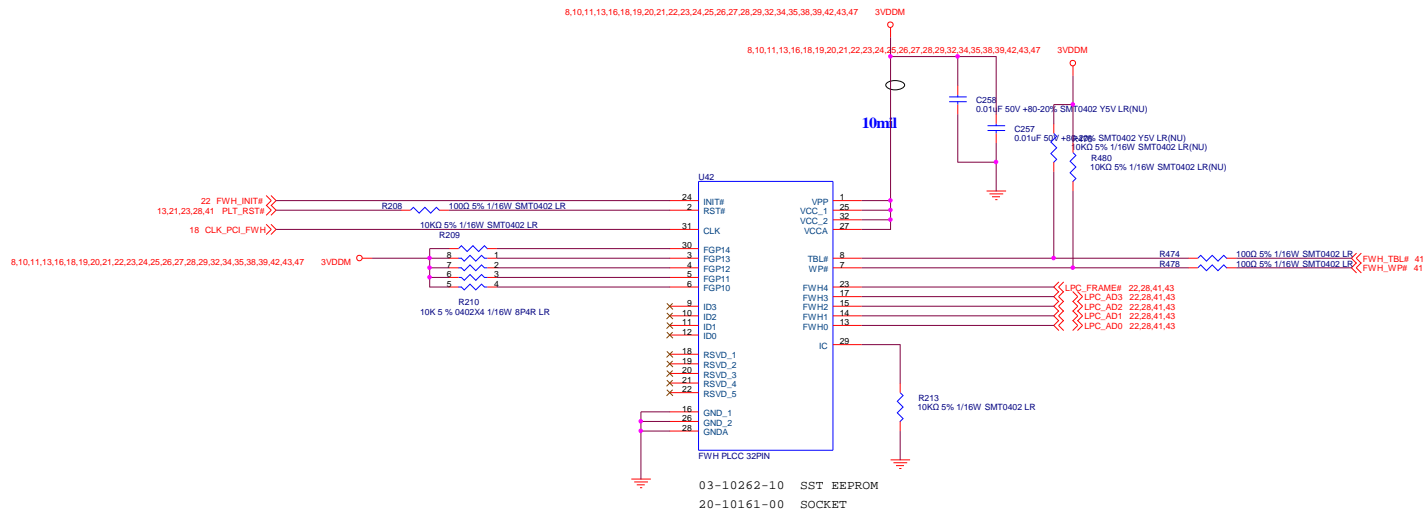
Trace:10mil, Spacing:10mil

## RESUME RESET

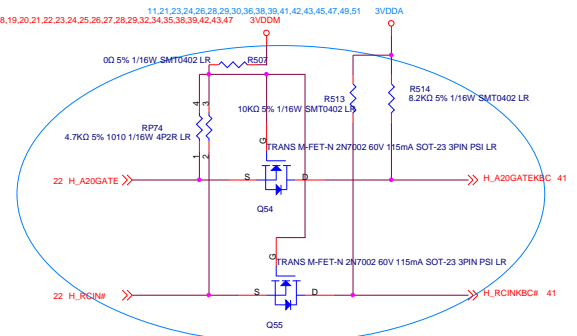
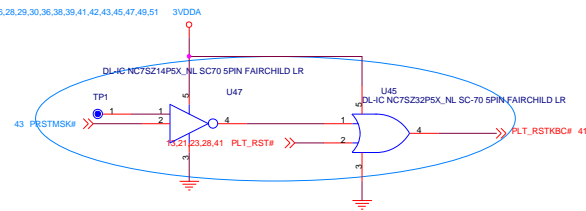


## NAPA Platfoem Power Good Circuit





Could be shorted if Bios  
disable PMU\_BLAJ# during  
S3-S5







## DIP SWITCH

8,10,11,13,16,18,19,20,21,22,23,24,25,26,27,28,29,32,34,35,38,39,40,43,47 3VDDM

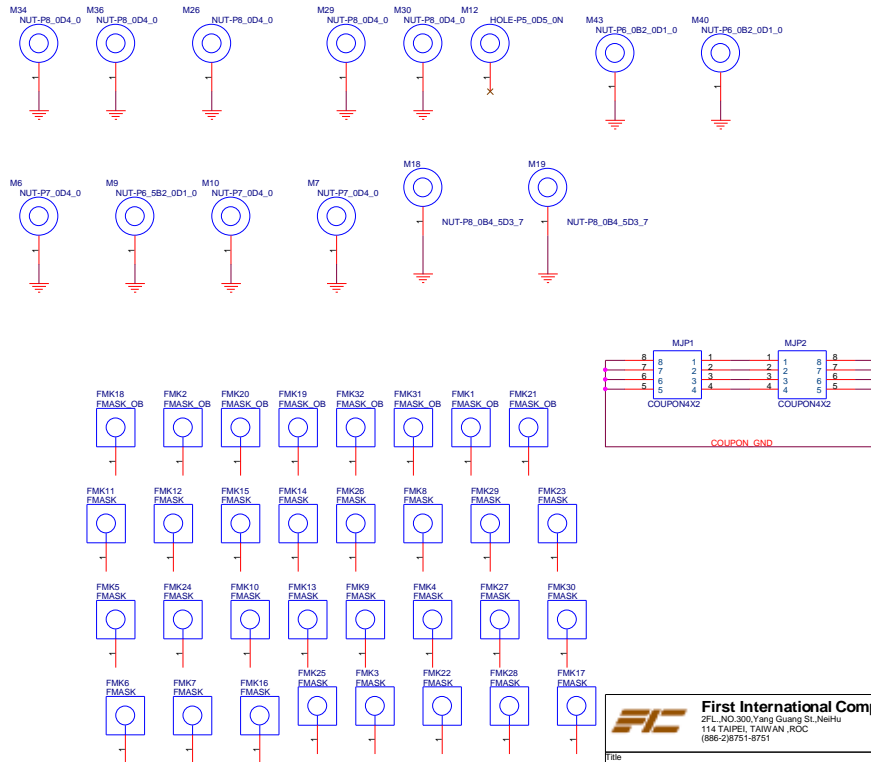
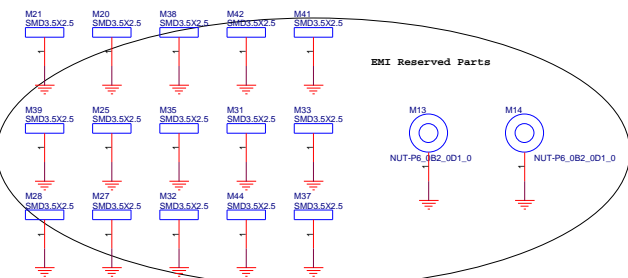
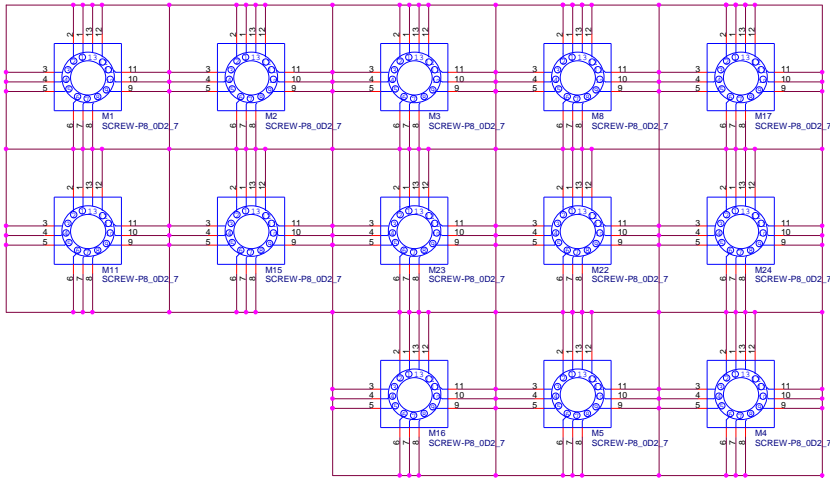
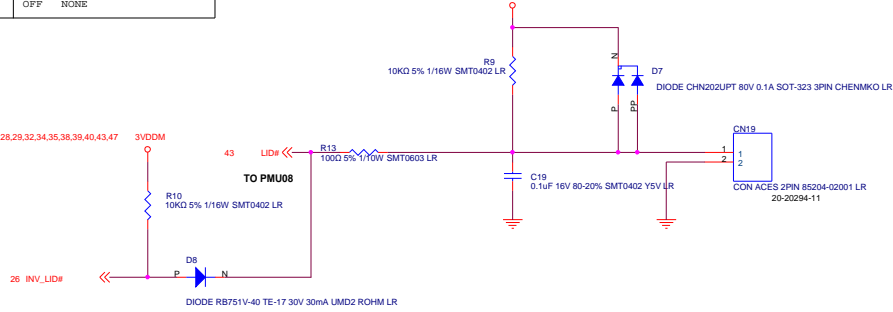


KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

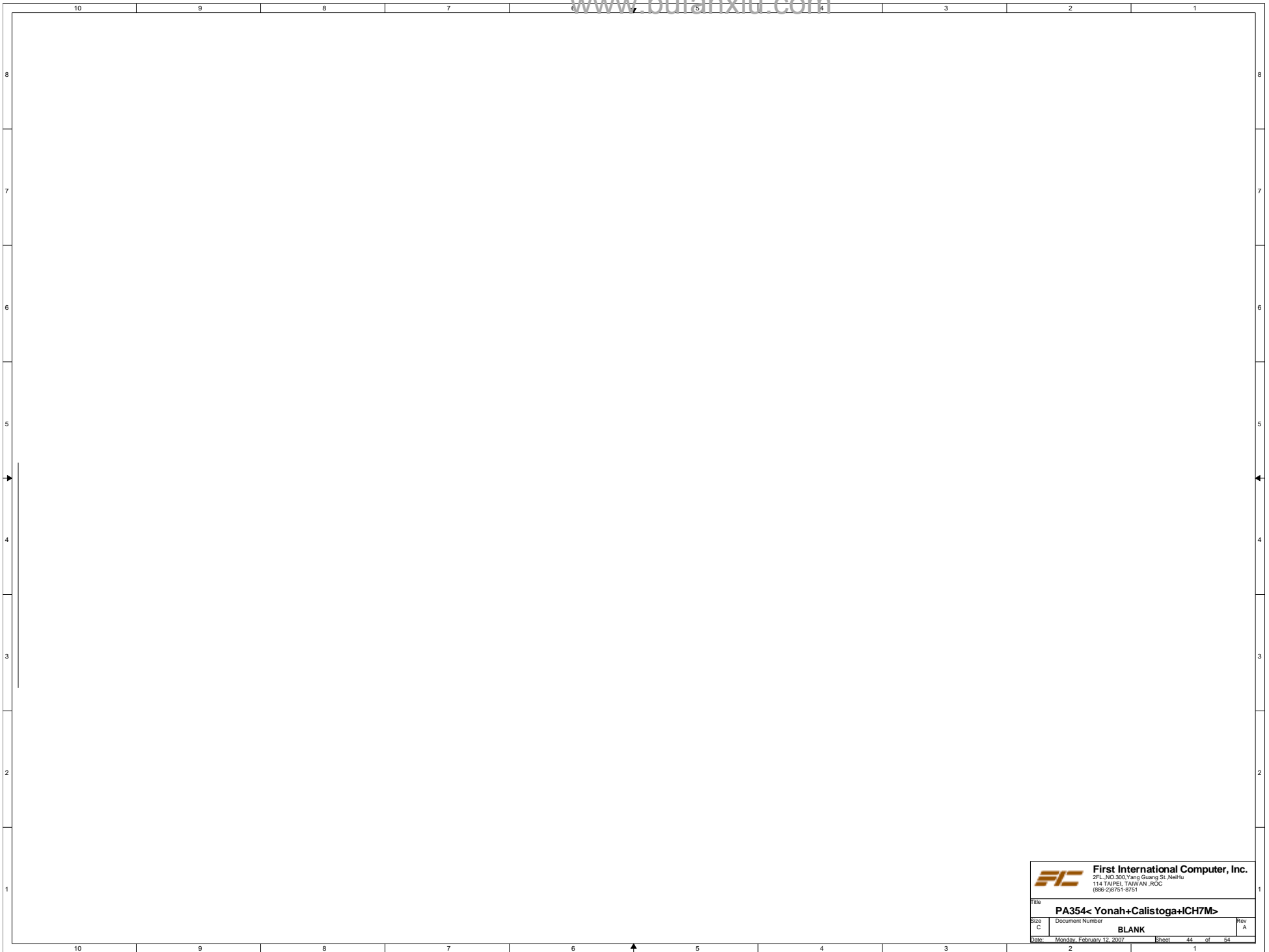
MB_ID0	ON	Reserved
	OFF	Reserved
LOGSEL	ON	Reserved
	OFF	Reserved
CMOS_CLEAR	ON	Reset RTC
	OFF	NONE


## LID Switch

11,21,23,24,26,28,29,30,36,38,39,40,41,43,45,47,49,5







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Title		PA354< Yonah+Calistoga+ICH7M>	
Size	Document Number	Rev	
C	BLANK	A	
Date	Monday, February 12, 2007	Sheet	44 of 54



## CHR Board BATTERY IN

### Close to PMU08

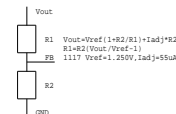
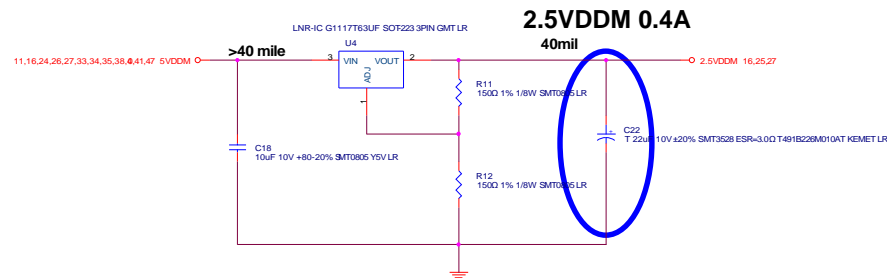
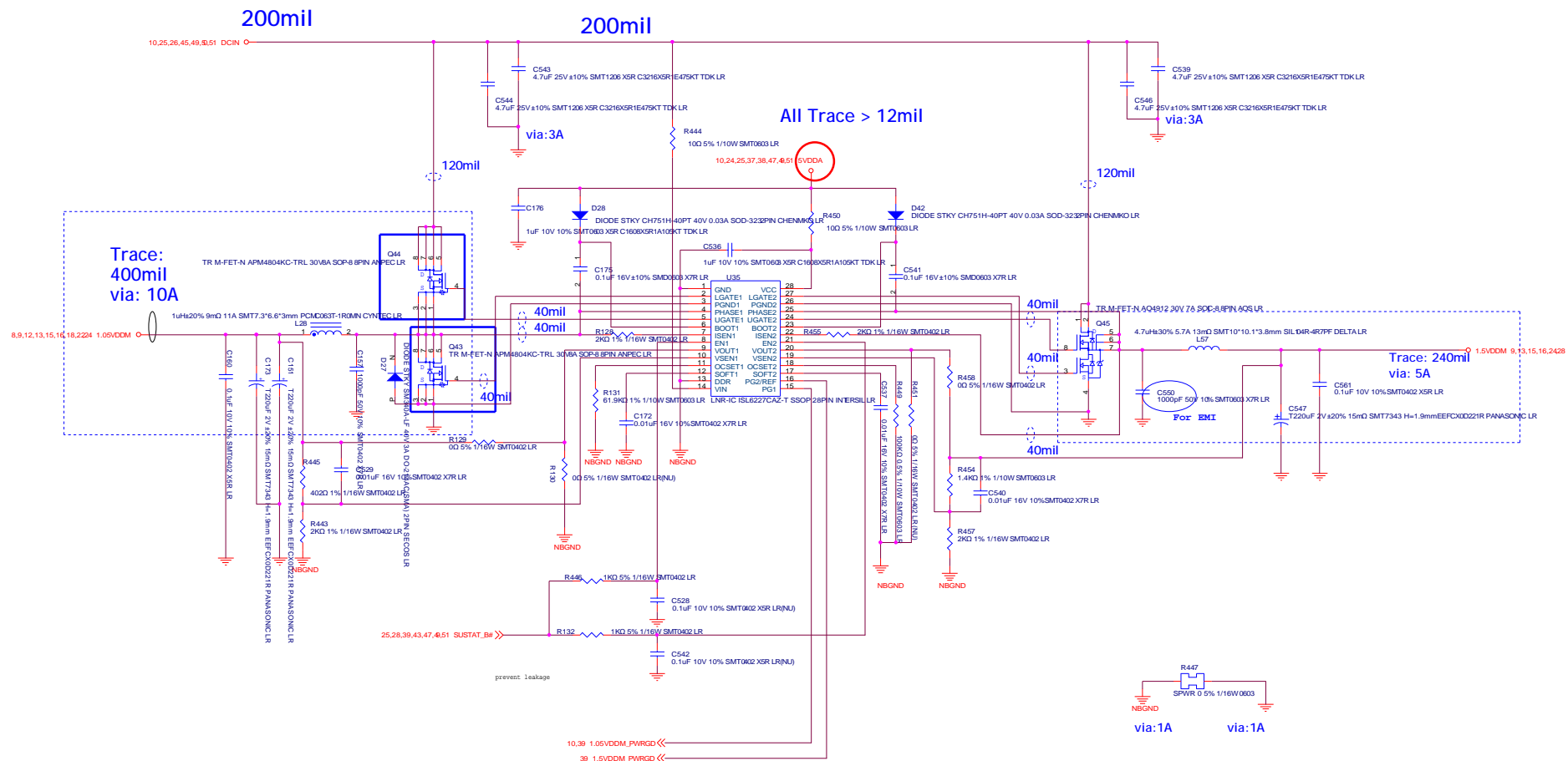
$8A = 320 \text{ MIL}$

8A=320 MIL

8A=320  
MIL

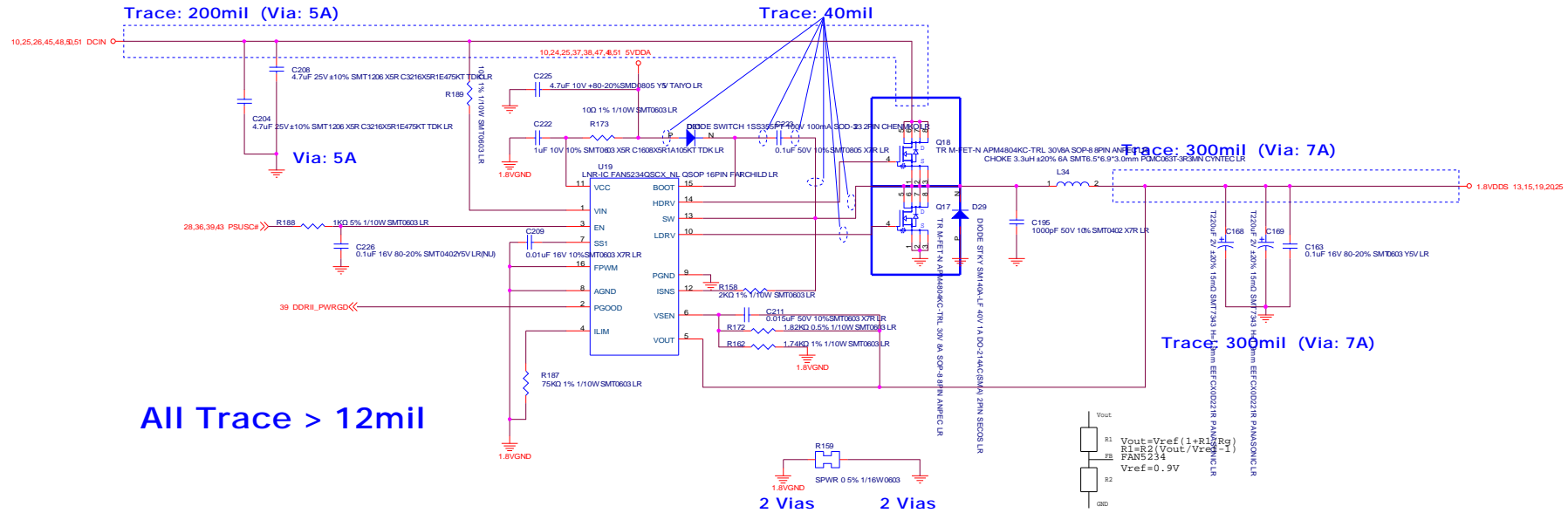
C10328-10801  
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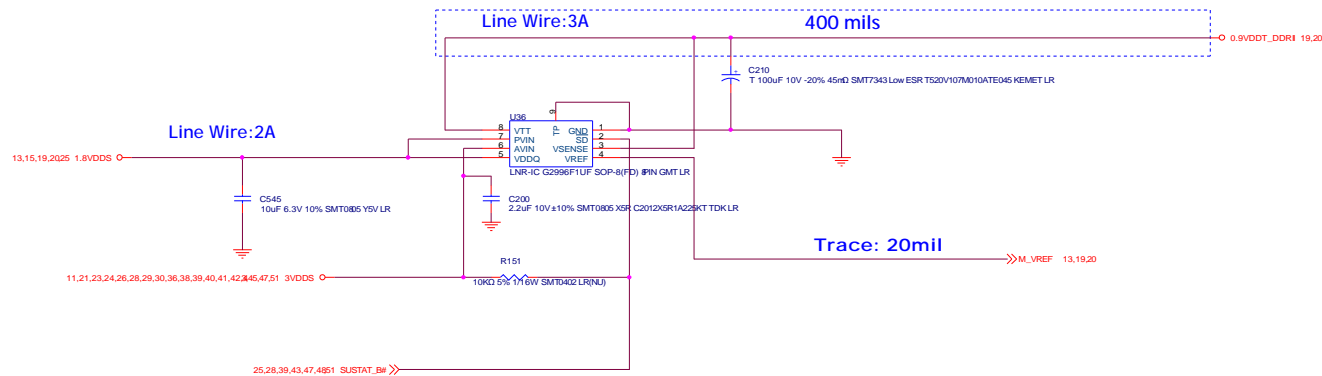


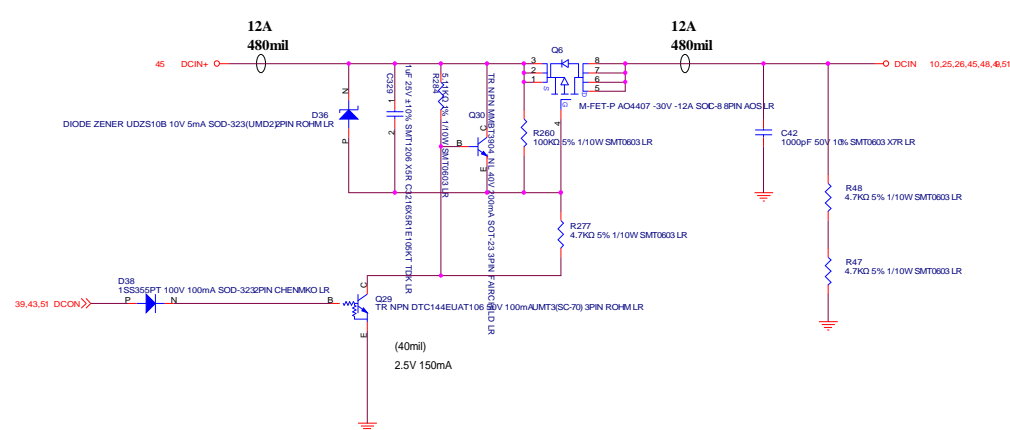
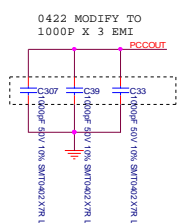
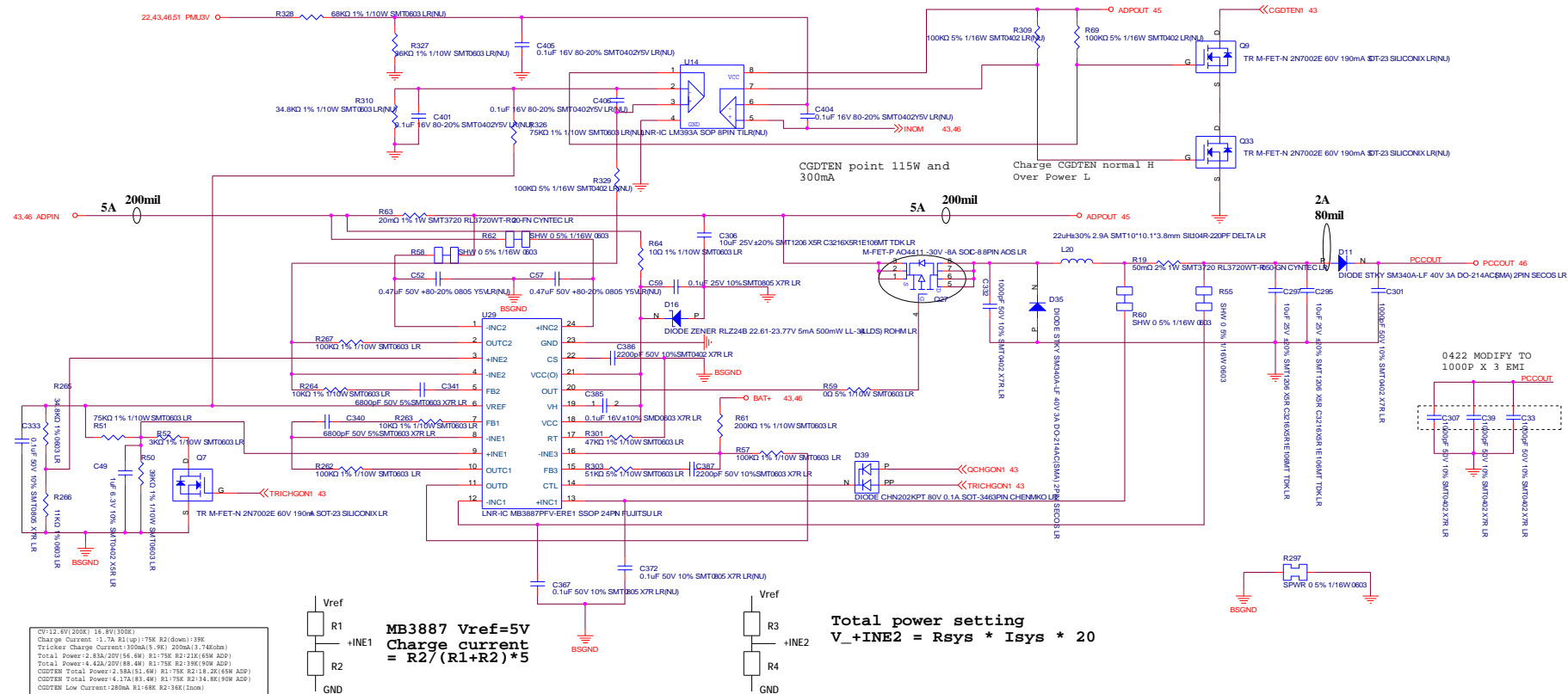


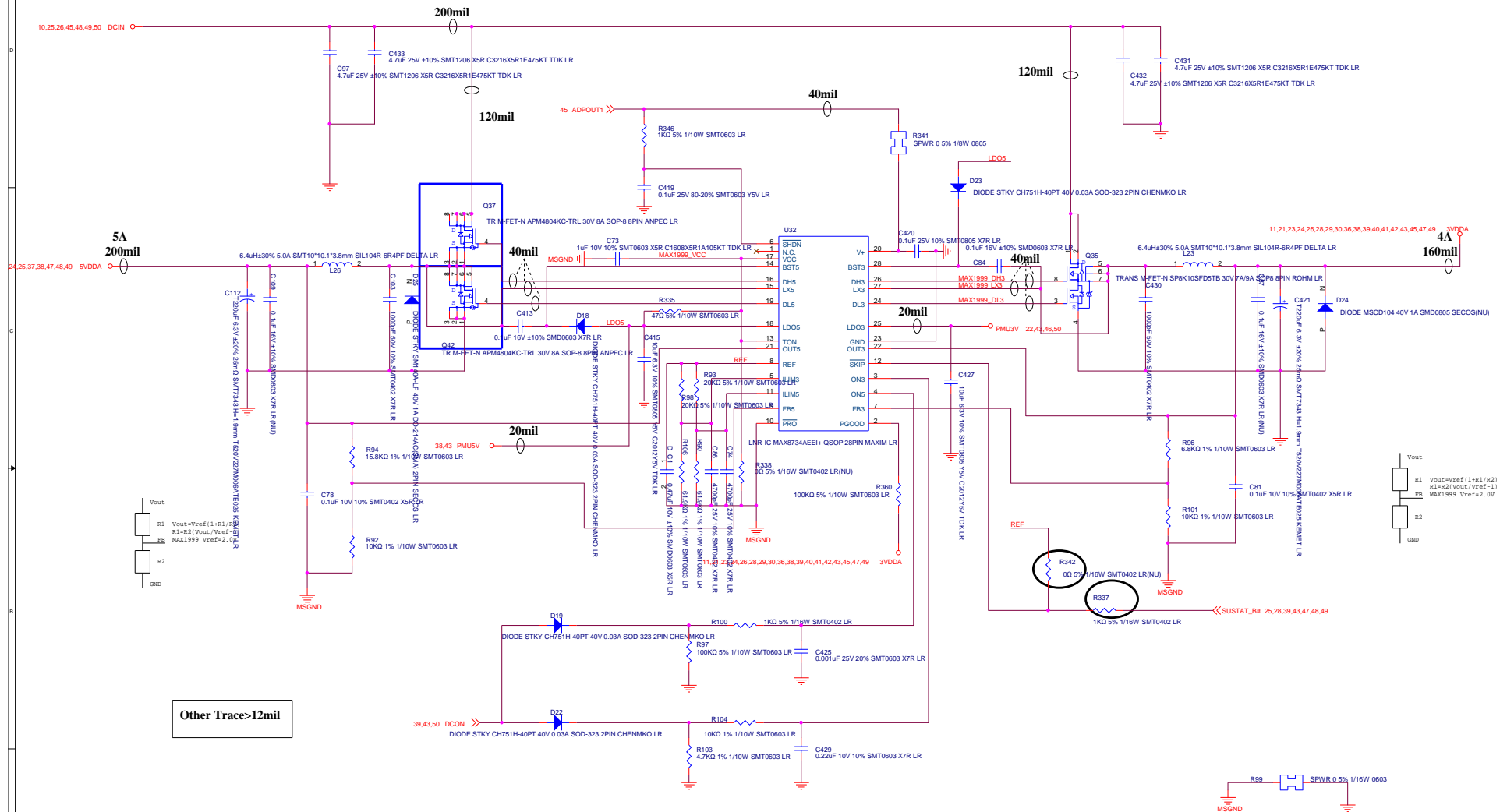
## DDRII Power

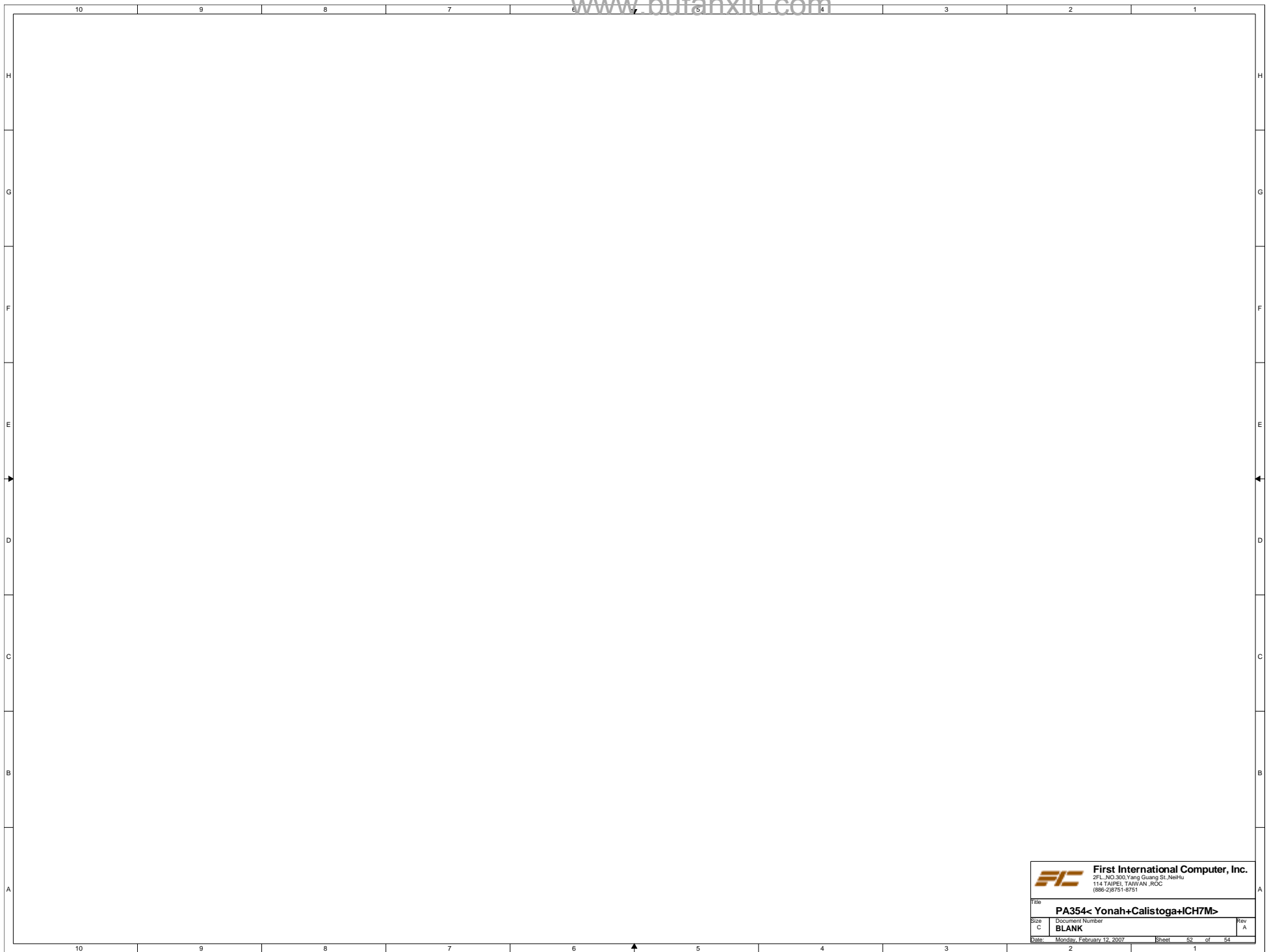


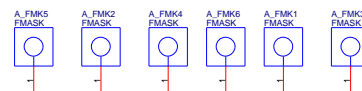
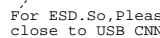
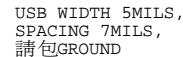
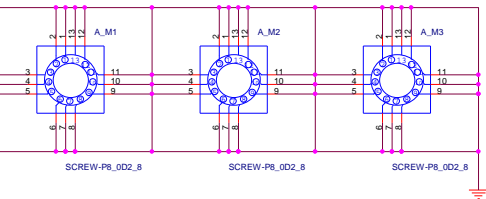
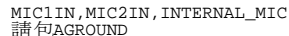
## DDRII Terminator Power











2/21 GND  
change AGND

